

BEST AVAILABLE COPY**AMENDMENT TO THE CLAIMS**

Please replace the claims with the following rewritten listing:

1. (Canceled)

2. (Currently Amended) ~~The~~An active matrix type display device ~~comprising:~~according to claim 1_____ a plurality of gate lines;_____ a plurality of data lines crossing said plurality of gate lines;_____ a plurality of pixel electrodes;_____ a thin film transistor disposed at each intersection between said plurality of gate lines and said plurality of data lines, and including a gate electrode and an active region, said gate electrode being connected to one of said plurality of gate lines, and said active region having a first region connected to one of said plurality of data lines and a second region connected to a corresponding one of said plurality of pixel electrodes; and_____ a gate line driver for sequentially applying a gate selection signal with a pulse-shaped voltage waveform to a selected one of said plurality of gate lines; wherein_____ said gate line driver causes a falling edge of said gate selection signal with said pulse-shaped voltage waveform to be smoother than a rising edge thereof;_____ wherein said gate selection signal requires at least a time $t/2$ to fall, where t is the time from when a first gate line assumes an unselected state to when subsequent second gate line assumed a selected state.

3. (Canceled)

4. (Currently Amended) ~~The~~An active matrix type display device ~~comprising:~~according to claim 1;_____ a plurality of gate lines;_____ a plurality of data lines crossing said plurality of gate lines;_____ a plurality of pixel electrodes;

a thin film transistor disposed at each intersection between said plurality of gate lines and said plurality of data lines, and including a gate electrode and an active region, said gate electrode being connected to one of said plurality of gate lines, and said active region having a first region connected to one of said plurality of data lines and a second region connected to a corresponding one of said plurality of pixel electrodes; and

a gate line driver for sequentially applying a gate selection signal with a pulse-shaped voltage waveform to a selected one of said plurality of gate lines; wherein said gate line driver causes a falling edge of said gate selection signal with said pulse-shaped voltage waveform to be smoother than a rising edge thereof;

wherein said gate line driver includes a gate buffer provided at a final stage and connected to a corresponding one of said plurality of gate lines,

said gate buffer includes a transistor having first and second regions of an active layer respectively connected to the ground and to said corresponding gate line, and

the condition, $2.5(R1+R2)*(C1+C2) < t < 5(R1+R2)*(C1+C2)$, is satisfied,

wherein

R1 represents a total resistance of said gate line and the gate electrodes of the thin film transistors connected to said gate line in a pixel region,

C1 represents a total capacitance of capacitors connected to said gate line in the pixel region and having said gate line as one electrode,

R2 represents a channel resistance of the transistor in said gate buffer,

C2 represents a capacitance of a capacitor formed by said active layer of the transistor in said gate buffer and the gate electrode of said transistor, and

t represents a flyback period in a horizontal scanning period.

5. (Original) The active matrix type display device according to claim 4, wherein a channel length L and a channel width W of the transistor in said gate buffer satisfy the condition $W/L < 1$.

6. (Currently Amended) ~~The~~ An active matrix type display device comprising; according to claim 1,

a plurality of gate lines;

_____ a plurality of data lines crossing said plurality of gate lines;
_____ a plurality of pixel electrodes;
_____ a thin film transistor disposed at each intersection between said plurality of gate lines and said plurality of data lines, and including a gate electrode and an active region, said gate electrode being connected to one of said plurality of gate lines, and said active region having a first region connected to one of said plurality of data lines and a second region connected to a corresponding one of said plurality of pixel electrodes; and
_____ a gate line driver for sequentially applying a gate selection signal with a pulse-shaped voltage waveform to a selected one of said plurality of gate lines; wherein
_____ said gate line driver causes a falling edge of said gate selection signal with said pulse-shaped voltage waveform to be smoother than a rising edge thereof;
_____ wherein, said gate line driver includes a gate buffer provided at a final stage and connected to a corresponding one of said plurality of gate lines,
_____ said gate buffer includes a transistor having first and second regions of an active layer respectively connected to the ground and to said corresponding gate line, and
_____ a channel length L and a channel width W of the transistor in said gate buffer satisfy the condition $W/L < 1$.

7. (Currently Amended) The An active matrix type display device comprising: according to claim 1;

_____ a plurality of gate lines;
_____ a plurality of data lines crossing said plurality of gate lines;
_____ a plurality of pixel electrodes;
_____ a thin film transistor disposed at each intersection between said plurality of gate lines and said plurality of data lines, and including a gate electrode and an active region, said gate electrode being connected to one of said plurality of gate lines, and said active region having a first region connected to one of said plurality of data lines and a second region connected to a corresponding one of said plurality of pixel electrodes; and
_____ a gate line driver for sequentially applying a gate selection signal with a pulse-shaped voltage waveform to a selected one of said plurality of gate lines; wherein

said gate line driver causes a falling edge of said gate selection signal with said pulse-shaped voltage waveform to be smoother than a rising edge thereof;

wherein, said gate line driver includes a gate buffer provided at a final stage and connected to a corresponding one of said plurality of gate lines,

said gate buffer includes a current supplying transistor having first and second regions of an active layer connected between a power source and said corresponding gate line, and a current discharging transistor having first and second regions of an active layer respectively connected to the ground and to said corresponding gate line, and

the ratio (channel width W) / (channel length L) of said current supplying transistor differs from the ratio (channel width W) / (channel length L) of said current discharging transistor.

8. (Original) The active matrix type display device according to claim 7, wherein

the condition, $2.5(R1+R2)*(C1+C2) < t < 5(R1+R2)*(C1+C2)$ is satisfied wherein

R1 represents a total resistance of said gate line and the gate electrodes of the thin film transistors connected to said gate line in a pixel region,

C1 represents a total capacitance of capacitors connected to said gate line in the pixel region and having said gate line as one electrode,

R2 represents a channel resistance of the current discharging transistor in said gate buffer,

C2 represents a capacitance of a capacitor formed by said active layer of the current discharging transistor in said gate buffer and the gate electrode thereof, and

t represents a flyback period in a horizontal scanning period.

9. (Original) The active matrix type display device according to claim 8, wherein the channel length L and the channel width W of the current discharging transistor in said gate buffer satisfy the condition $W/L < 1$.

10. (Original) The active matrix type display device according to claim 8, wherein the condition that the ratio of (the ratio W/L of said current supplying transistor) / (the ratio W/L of said current discharging transistor) is greater than 1 is satisfied.

11. (Original) The active matrix type display device according to claim 8, wherein the condition that the ratio of (the ratio W/L of said current supplying transistor) / (the ratio of said current discharging transistor) is greater than 5 is satisfied.

12. (Canceled)

13. (Currently Amended) ~~The~~An active matrix type display device ~~comprising according to claim 12~~

~~_____ a plurality of gate lines;~~

~~_____ a plurality of data lines crossing said plurality of gate lines;~~

~~_____ a plurality of pixel electrodes;~~

~~_____ a thin film transistor disposed at each intersection between said plurality of gate lines and said plurality of data lines, and including a gate electrode and an active region, said gate electrode being connected to one of said plurality of gate lines, and said active region having a first region connected to one of said plurality of data lines and a second region connected to a corresponding one of said plurality of pixel electrodes; and~~

~~_____ a gate line driver for sequentially applying a gate selection signal with a pulse-shaped voltage waveform to a selected one of said plurality of gate lines; wherein~~

~~_____ said gate line driver causes a falling time of said gate selection signal to be longer than a rising time thereof;~~

~~_____ wherein said gate selection signal requires at least a time $t/2$ to fall, where t is a time from when a first gate line assumes an unselected state to when a subsequent second gate line assumes a selected state.~~

14. (Canceled)

15. (Currently Amended) ~~The~~ An active matrix type display device comprising:
according to claim 12;

_____ a plurality of gate lines;

_____ a plurality of data lines crossing said plurality of gate lines;

_____ a plurality of pixel electrodes;

_____ a thin film transistor disposed at each intersection between said plurality of gate lines and said plurality of data lines, and including a gate electrode and an active region, said gate electrode being connected to one of said plurality of gate lines, and said active region having a first region connected to one of said plurality of data lines and a second region connected to a corresponding one of said plurality of pixel electrodes; and

_____ a gate line driver for sequentially applying a gate selection signal with a pulse-shaped voltage waveform to a selected one of said plurality of gate lines; wherein
_____ said gate line driver causes a falling time of said gate selection signal to be longer than a rising time thereof;

_____ wherein said gate line driver includes a gate buffer provided at a final stage and connected to a corresponding one of said plurality of gate lines,

_____ said gate buffer includes a transistor having first and second regions of an active layer respectively connected to the ground and to said corresponding gate line, and

_____ the condition, $2.5(R1+R2)*(C1+C2) < t < 5(R1+R2)*(C1+C2)$, is satisfied,
wherein

_____ R1 represents a total resistance of said gate line and the gate electrodes of the thin film transistors connected to said gate line in a pixel region,

_____ C1 represents a total capacitance of capacitors connected to said gate line in the pixel region and having said gate line as one electrode,

_____ R2 represents a channel resistance of the transistor in said gate buffer,

_____ C2 represents a capacitance of a capacitor formed by said active layer of the transistor in said gate buffer and the gate electrode of said transistor, and

_____ t represents a flyback period in a horizontal scanning period.

16. (Original) The active matrix type display device according to claim 15, wherein a channel length L and a channel width W of the transistor in said gate buffer satisfy the condition $W/L < 1$.

17. (Currently Amended) The Δn active matrix type display device comprising:
according to claim 12;

_____ a plurality of gate lines;

_____ a plurality of data lines crossing said plurality of gate lines;

_____ a plurality of pixel electrodes;

_____ a thin film transistor disposed at each intersection between said plurality of gate lines and said plurality of data lines, and including a gate electrode and an active region, said gate electrode being connected to one of said plurality of gate lines, and said active region having a first region connected to one of said plurality of data lines and a second region connected to a corresponding one of said plurality of pixel electrodes; and

_____ a gate line driver for sequentially applying a gate selection signal with a pulse-shaped voltage waveform to a selected one of said plurality of gate lines; wherein
_____ said gate line driver causes a falling time of said gate selection signal to be longer than a rising time thereof;

_____ wherein, said gate line driver includes a gate buffer provided at a final stage and connected to a corresponding one of said plurality of gate lines,

_____ said gate buffer includes a transistor having first and second regions of an active layer respectively connected to the ground and to said corresponding gate line, and

_____ a channel length L and a channel width W of the transistor in said gate buffer satisfy the condition $W/L < 1$.

18. (Currently Amended) The Δn active matrix type display device comprising:
according to claim 12;

_____ a plurality of gate lines;

_____ a plurality of data lines crossing said plurality of gate lines;

_____ a plurality of pixel electrodes;

a thin film transistor disposed at each intersection between said plurality of gate lines and said plurality of data lines, and including a gate electrode and an active region, said gate electrode being connected to one of said plurality of gate lines, and said active region having a first region connected to one of said plurality of data lines and a second region connected to a corresponding one of said plurality of pixel electrodes; and

a gate line driver for sequentially applying a gate selection signal with a pulse-shaped voltage waveform to a selected one of said plurality of gate lines; wherein said gate line driver causes a falling time of said gate selection signal to be longer than a rising time thereof;

wherein, said gate line driver included a gate buffer provided at a final stage and connected to a corresponding one of said plurality of gate lines,

said gate buffer includes a current supplying transistor having first and second regions of an active layer connected between a power source and said corresponding gate line, and a current discharging transistor having first and second regions of an active layer respectively connected to the ground and to said corresponding gate line, and

the ratio (channel width W) / (channel length L) of said current supplying transistor differs from the ratio (channel width W) / (channel length L) of said current discharging transistor.

19. (Original) The active matrix type display device according to claim 18, wherein the condition, $2.5(R1+R2)*(C1+C2) < t < 5(R1+R2)*(C1+C2)$, is satisfied wherein

R1 represents a total resistance of said gate line and the gate electrodes of the thin film transistors connected to said gate line in a pixel region,

C1 represents a total capacitance of capacitors connected to said gate line in the pixel region and having said gate line as one electrode,

R2 represents a channel resistance of the current discharging transistor in said gate buffer,

C2 represents a capacitance of a capacitor formed by said active layer of the current discharging transistor in said gate buffer and the gate electrode thereof, and

t represents a flyback period in a horizontal scanning period.

20. (Original) The active matrix type display device according to claim 18, wherein the channel length L and the channel width W of the current discharging transistor in said gate buffer satisfy the condition $W/L < 1$.

21. (Original) The active matrix type display device according to claim 18, wherein the condition that the ratio of (the ratio W/L of said current supplying transistor) / (the ratio W/L of said current discharging transistor) is greater than 1 is satisfied.

22. (Original) The active matrix type display device according to claim 18, wherein the condition that the ratio of (the ratio W/L of said current supplying transistor) / (the ratio W/L of said current discharging transistor) is greater than 5 is satisfied.

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

☐ BLACK BORDERS

☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES

☒ FADED TEXT OR DRAWING

☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING

☐ SKEWED/SLANTED IMAGES

☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS

☐ GRAY SCALE DOCUMENTS

☐ LINES OR MARKS ON ORIGINAL DOCUMENT

☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY

☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.